AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

Please cancel claims 5, 9, 11, 12, 15 and 20 without prejudice.

1. (CURRENTLY AMENDED) A method of synchronizing a phase lock loop to an intermittent clock signal, the method comprising the steps of:

(A) seeking to acquire phase lock of the phase lock loop with the intermittent clock signal during a plurality of first periods of the intermittent clock signal when the intermittent clock signal is present;

(B) timing a duration for each of the first periods; ~~and~~

(C) holding the phase lock loop in a free-running state in advance of and during a plurality of second periods read from a header region on an optical disk when the intermittent clock signal is absent in response to the duration indicating an end to one of the first periods;

(D) identifying re-emergence of the intermittent clock signal; and

(E) seeking to acquire phase lock only after re-emergence of the intermittent clock signal has been validated.

2. (PREVIOUSLY PRESENTED) The method according to claim 1, further comprising the step of:

acquiring frequency lock in an asynchronous mode.

3. (ORIGINAL) The method according to claim 1, wherein the intermittent clock signal is derived from a geometric eccentricity associated with a track on an optical disc and the geometric eccentricity is interspersed by regularly spaced header regions that disrupt the geometric eccentricity.

4. (CURRENTLY AMENDED) ~~The method according to claim 1, wherein step (C) comprises the sub-step of:~~ A method of synchronizing a phase lock loop to an intermittent clock signal, the method comprising the steps of:

(A) seeking to acquire phase lock of the phase lock loop with the intermittent clock signal during a plurality of first periods of the intermittent clock signal when the intermittent clock signal is present;

(B) timing a duration for each of the first periods; and

(C) holding the phase lock loop in a free-running state during a plurality of second periods when the intermittent clock signal is absent in response to the duration indicating an end to one of the first periods, wherein ~~placing~~ the phase lock loop is placed in the free-running state in advance of reading a header region on an optical disk in response to the duration.

5. (CANCELED)

6. (CURRENTLY AMENDED) A method of synchronizing a phase lock loop to an intermittent clock signal, the method comprising the steps of:

(A) seeking to acquire phase lock during periods of the intermittent clock signal;

(B) holding the phase lock loop in a free-running state during periods when the intermittent clock signal is absent; ~~and~~

(C) estimating a signal envelope for the intermittent clock signal; and

(D) bandpass filtering an input signal to generate a plurality of spikes indicative of a transition for a header region on an optical disk.

7. (CURRENTLY AMENDED) The method according to claim ~~20~~ 6, further comprising the step of:

identifying a relative signal level polarity between a first spike of the spikes and a successive spike of the spikes to identify a requirement for a phase reversal.

8. (ORIGINAL) The method according to claim 6, further comprising:

filtering the intermittent clock signal in a low pass filter to generate an adaptive slice level signal capable of tracking residual near-DC variations in the intermittent clock signal.

9. (CANCELED)

10. (CURRENTLY AMENDED) A system comprising:

a phase lock loop arranged to receive an intermittent clock signal to which the phase lock loop is to be synchronized, wherein the intermittent clock signal is derived from a geometric eccentricity associated with a track on an optical disc and the geometric eccentricity is interspersed by regularly spaced header regions that disrupt the geometric eccentricity and which each define a data sector; and

a control circuit comprising a counter arranged to time the intermittent clock signal during each of the data sectors, the control circuit configured to (i) maintain operational control of the phase lock loop, (ii) determine a plurality of first periods of time when the intermittent clock signal is stable, (iii) selectively maintain the phase lock loop in a phase acquisition state during the first periods of time, and (iv) force the phase lock loop to enter a free-running state during a plurality of second periods of time when the intermittent clock signal is absent in response to time within each of the data sectors and in advance of an arrival of each of the header regions.

11. (CANCELED)

12. (CANCELED)

13. (PREVIOUSLY PRESENTED) A system comprising:

a phase lock loop arranged to receive an intermittent clock signal to which the phase lock loop is to be synchronized;

a control circuit configured to (i) maintain operational control of the phase lock loop, (ii) determine periods of time when the intermittent clocking signal is stable, (iii) selectively maintain the phase lock loop in a phase acquisition state during the periods of time and (iv) force the phase lock loop to enter a free-running state during periods of time when the intermittent clock signal is absent; and

a bandpass filter configured to filter an input signal to generate the intermittent clock signal and a plurality of spikes indicative of a header region of an optical disk.

14. (PREVIOUSLY PRESENTED) The system of claim 27, wherein the comparator arrangement comprises a first and a second comparators configured to process opposite signal senses from the signal envelope, the first and the second comparators each providing an output to a controller arranged to identify a relative signal level polarity between the first spike and a successive spike of the spikes to identify a requirement for a phase reversal in the phase lock loop.

15. (CANCELED)

16. (CANCELED)

17. (CANCELED)

18. (CANCELED)

19. (CANCELED)

20. (CANCELED)

21. (CURRENTLY AMENDED) The method according to claim ~~20~~ 6, further comprising the step of:

amplifying the signal envelope and the spikes to scale the spikes relative to the signal envelope to differentiate the signal envelope from the spikes.

22. (PREVIOUSLY PRESENTED) The method according to claim 21, further comprising the step of:

defining a threshold exceeding the signal envelope.

23. (PREVIOUSLY PRESENTED) The method according to claim 22, further comprising the step of:

identifying commencement of the header region by equating a first transition of the spikes through the threshold as being indicative of the header region.

24. (PREVIOUSLY PRESENTED) The system of claim 13, further comprising:

a top hold feedback circuit arranged to estimate a signal envelope for the intermittent clock signal.

25. (PREVIOUSLY PRESENTED) The system of claim 24, further comprising:

an amplifier configured to amplify the signal envelope and the spikes, to scale the spikes relative to the signal envelope to differentiate the signal envelope from the spikes.

26. (PREVIOUSLY PRESENTED) The system of claim 24, further comprising:

a data slicing circuit configured to define a threshold exceeding the signal envelope.

27. (PREVIOUSLY PRESENTED) The system of claim 26, further comprising:

a comparator arrangement configured to identify commencement of the header region by equating a first spike of the spikes transitioning through the threshold as being indicative of the header region.

28. (PREVIOUSLY PRESENTED) The system of claim 13, further comprising:

an array of photodiodes adapted to recover an input signal representation from an optical disc containing data segments interspersed with the header regions.